

SYETEM BUS 431

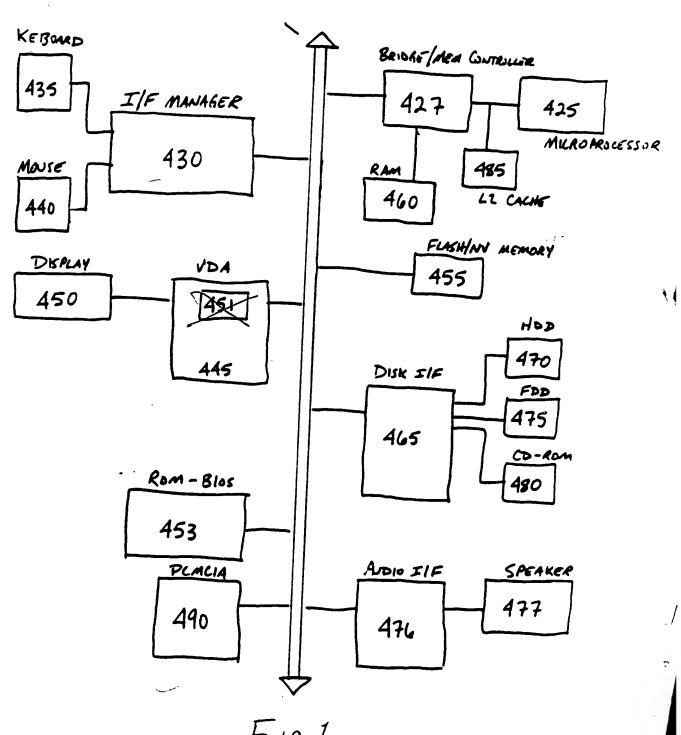


FIG 1



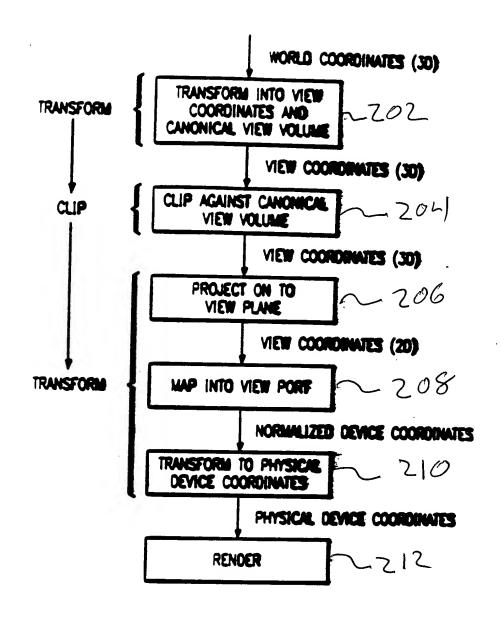


FIG. 2



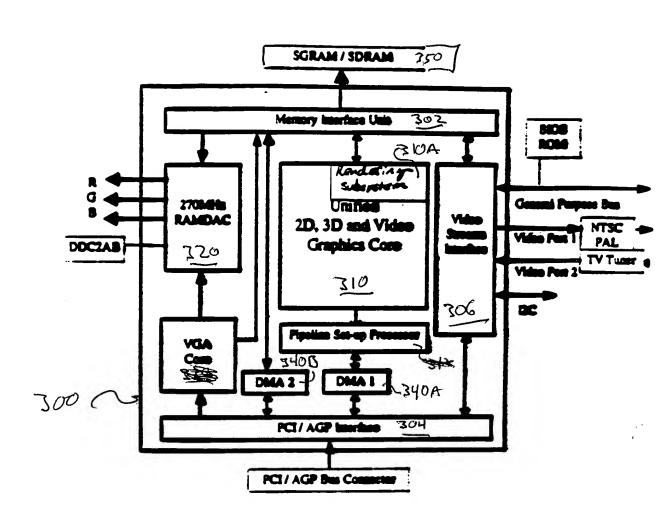


Figure 3



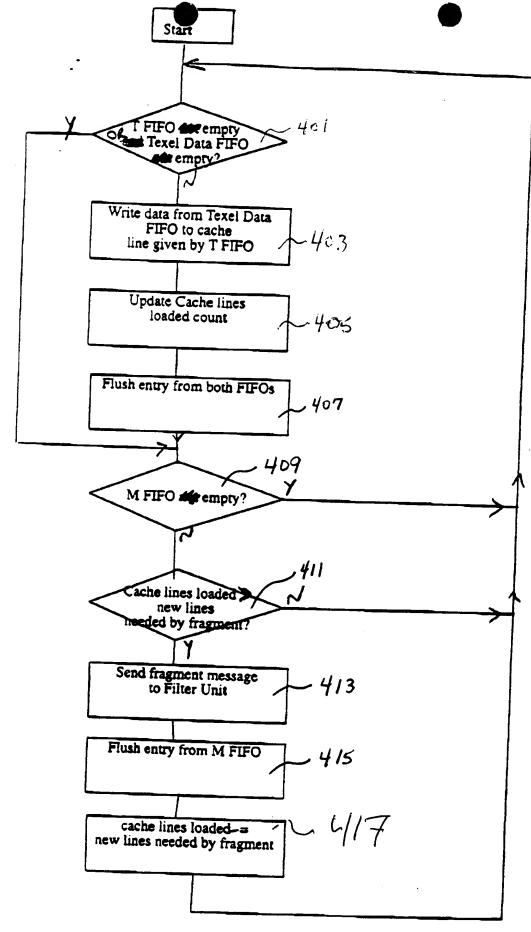


FIG. 4A



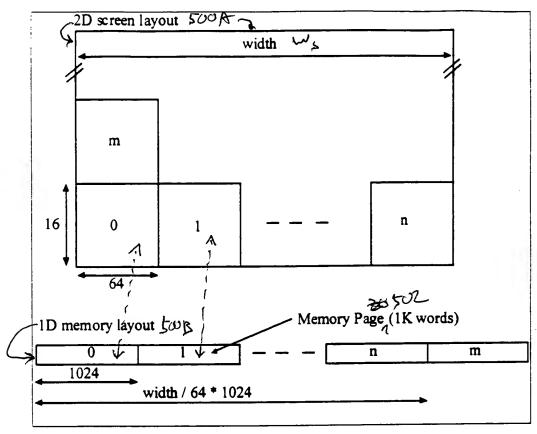


Fig. 5

-	.) .			(CO-1)	Texe		255. Shared	AT TO	APE	1 9 2003 E
32b 16b 17 8b		$-\frac{1}{\sqrt{\frac{5}{N}}}$	90	2	T0 (0,2)	(0,3)	(0,4)		1	
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32 bit texels in memory word 16 bit texels in memory word 8 bit texels in memory word			To	(2,1)	T0 (2,2)	T2 (2,3)	T0 (2,4)		exmic	_
ory wo	5		TI	(3,1)	T1 (3,2)	T3 (3,3)	T1 (3,4)	\	7	
nd (2/18)	<u> </u>		T0(4,0)	(4 <u>/</u> 1)	T0 (4,2)	T2 (4,3)	T0 (4,4)			•
- P 0		,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	(5,0)	T3 (5,1)	T1 (5,2)	T3 (5,3)	T1 (5,4)		2	
			T0 (6,0)	(6,1)	T0 (6,2)	T2 (6,3)	T0 (6,4)		8	
			(7,0)	(1,1) EI	T1 (7,2)	T3 (7,3)	T1 (7,4)			
			T0 (8,0)	T2 (8,1)	T0 (8,2)	T2 (8,3)	T0 (8,4)	-		
		!	T1 (9,0)	T3 (9,1)	T1 (9,2)	T3 (9,3)	T1 (9,4)	-		
	-							— Э		

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Linear or Patch64 Memory Layouts

120 112		88	80	72	64	56	(1,		32	24	(0,	0) 8	_
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DIES per te	zei Cim	-14 1-	ンコ										
	xel Chy or			- 72	64	56	48	40	32	24	16_	8	
120 112	104 96	88	80 4									<u>8</u>	0)
	•		80 4	(4,		56		(2,		(1, 0		(0,	0
(7, 0)	(6, 0)	(5, 0	80 \$									(0,	0)
(7, 0)	(6, 0)	(5, 0	80 \$									(0,	0)
(7, 0)	104 96 (6,0)	(5, 0	80 \$		0)	(3,	0)	(2,	0)	(1, ((0,	0)

FIG. 7A

Patch32_2 or Patch2 Memory Layouts

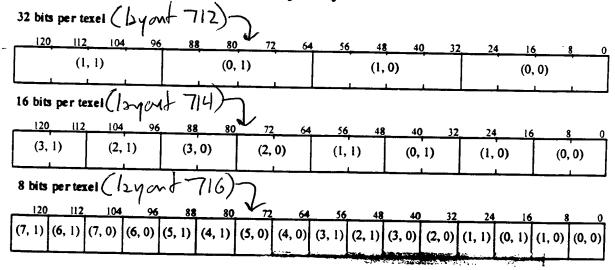
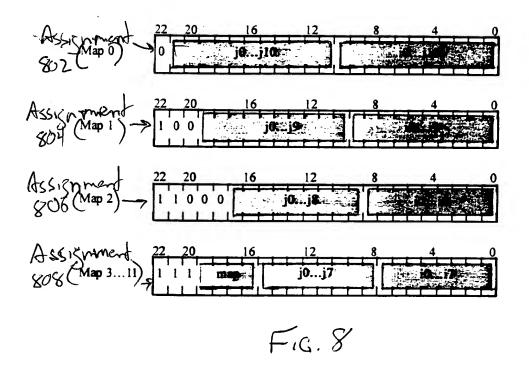


Fig. 7B







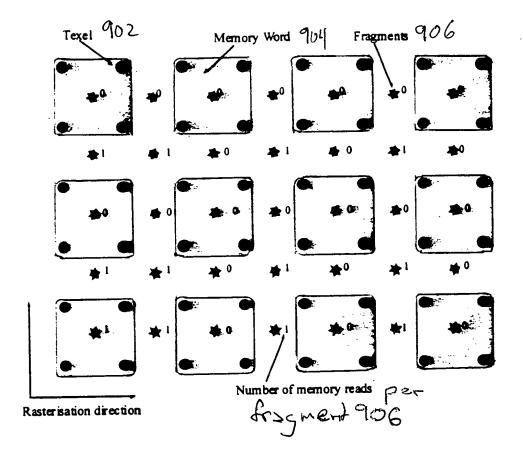


Fig. 9

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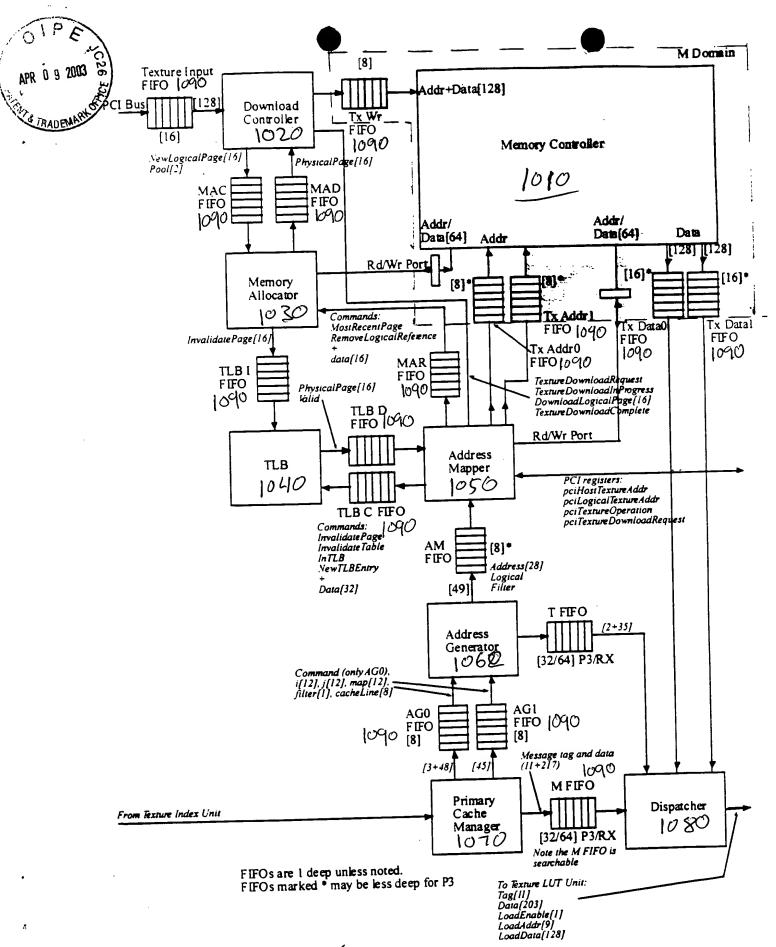


Fig. 10

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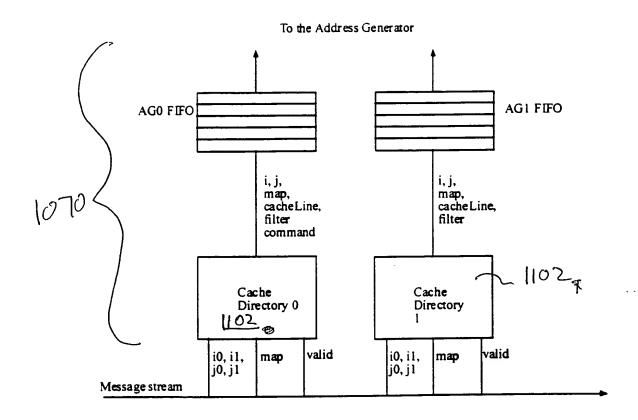


FIG. 11

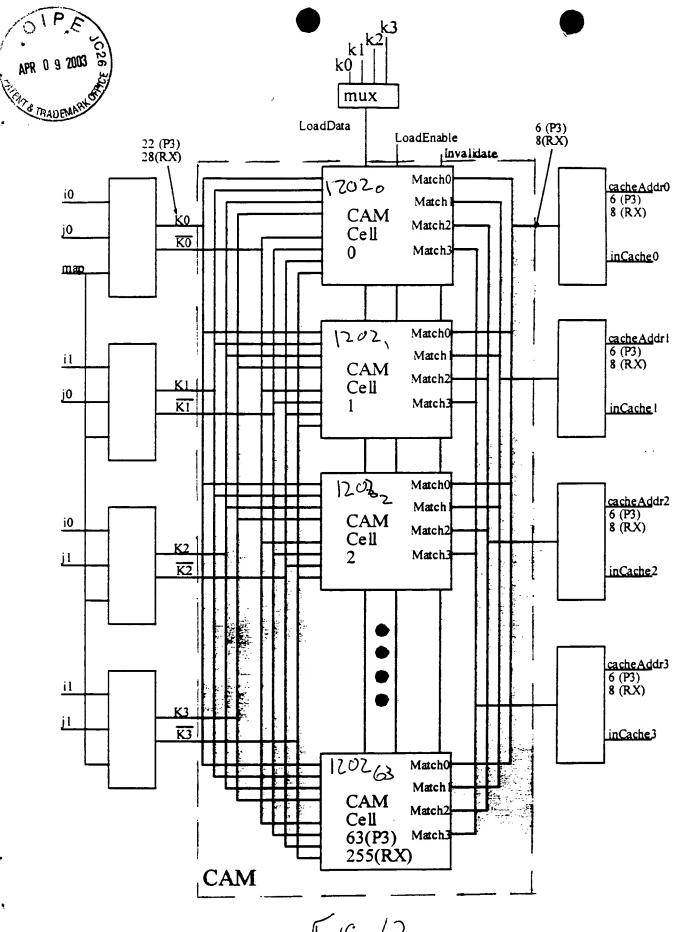
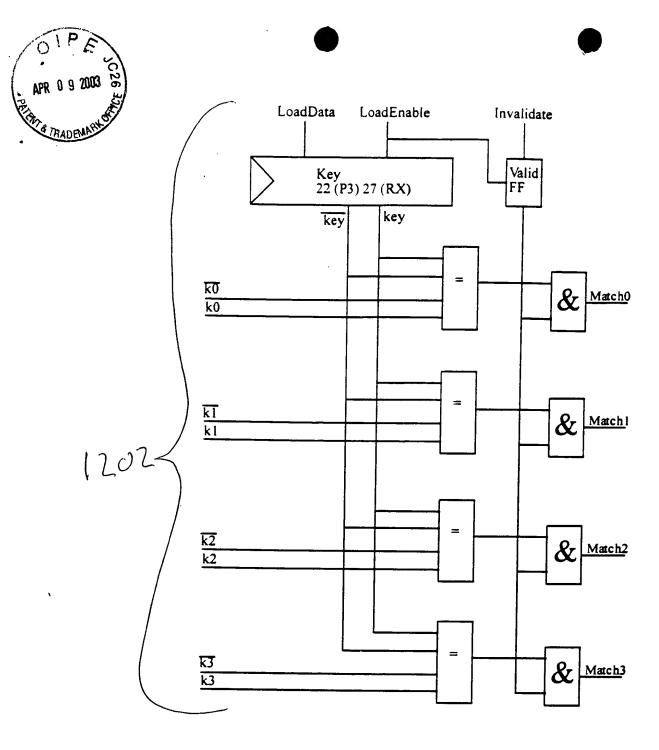


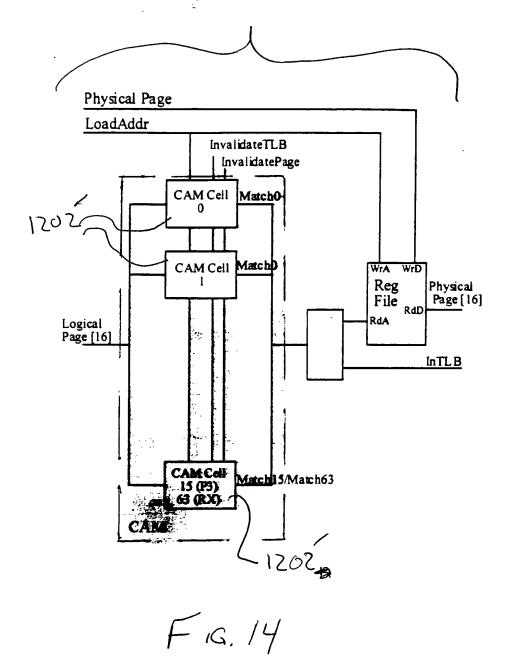
Fig /2

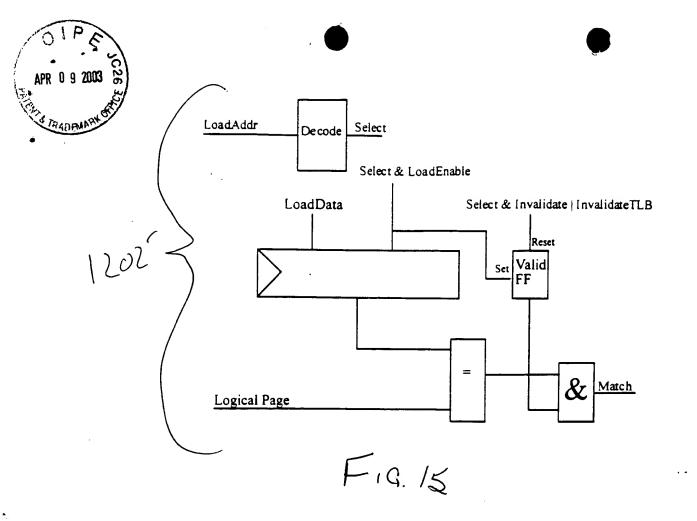


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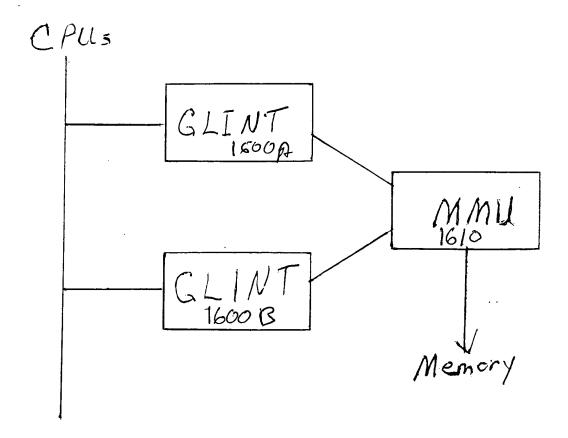


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